WHAT IS CLAIMED IS:

1. A level shift circuit comprising:

a level shift basic circuit for translating an input signal to an output signal which has a difference of a voltage between a first power supply and a second power supply having a lower voltage than that of the first power supply; and

a control circuit including a first circuit for disconnecting a feed-through current path in said level shift basic circuit between the first power supply and the second power supply in response to a first control input, and a second circuit for fixing a voltage of an output node from which the output signal is output in response to a second control input.

2. The level shift circuit of claim 1, wherein said level shift basic circuit includes:

a first transistor having a first conduction channel, interposed between the first power supply and a first node, and having a gate terminal receiving a second node;

a second transistor having the first conduction channel, interposed between the first power supply and the second node, and having a gate terminal receiving the first node;

a third transistor having a second conduction channel, interposed between the second node and a third node, and having a gate terminal controlled in response to a first input signal; and

a fourth transistor having the second conduction channel, interposed between the first node and a fourth node, and having a gate terminal controlled in response to a second input signal,

wherein said first circuit disconnects a feed-through current path between both the first node and the second node and the second power supply in response to the first control input, and

wherein at least one of the first node and the second node is used as the output

node.

3. The level shift circuit of claim 2, wherein the first conduction channel is a p-type conduction channel and the second conduction channel is an n-type conduction channel.

4. The level shift circuit of claim 2, wherein said first circuit comprises an n-MOS transistor, said n-MOS transistor is interposed between both the third node and the fourth node and the second power supply, and a gate terminal of said n-MOS transistor receives the first control input.

5. The level shift circuit of claim 2, wherein said first circuit comprises two n-MOS transistors, said two n-MOS transistors are interposed both between the third node and the second power supply and between the fourth node and the second power supply respectively, and a gate terminal of each of said two n-MOS transistors receives the first control input.

6. The level shift circuit of claim 2, wherein the third node and the fourth node are connected to the second power supply,

wherein said first circuit comprises a first two-input NOR and a second two-input NOR,

wherein one input of said first two-input NOR receives the first control input, the other input of said first two-input NOR receives the first input signal and an output of said first two-input NOR is connected to the gate terminal of said third transistor, and

wherein one input of said second two-input NOR receives the first control input,

the other input of said second two-input NOR receives the second input signal and an output of said second two-input NOR is connected to the gate terminal of said fourth transistor.

7. The level shift circuit of claim 2, wherein said second circuit precharges at least one of the first node and the second node in response to the second control input.

8. The level shift circuit of claim 2, wherein said second circuit comprises two p-MOS transistors, said two p-MOS transistors are interposed both between the first power supply and the first node and between the first power supply and the second node respectively, and a gate terminal of each of said two p-MOS transistors receives the second control input.

9. The level shift circuit of claim 8, wherein the first control input is controlled so that the feed-through current path is disconnected while the first input signal and the second input signal are changing.

10. The level shift circuit of claim 9, wherein the second control input is controlled so that said second circuit fixes the voltages of the first node and the second node while the first control input is controlled so that the feed-through current path is disconnected.

11. The level shift circuit of claim 1, wherein said control circuit is provided for a plurality of said level shift basic circuit.